PRESIDENCY COLLEGE
(AUTONOMOUS)
AFFILIATED TO BENGALURU CITY UNIVERSITY, APPROVED BY AICTE, DELHI & RECOGNISED BY THE GOVT. OF KARNATAKA
RE-ACCREDITED BY NAAC WITH 'A+' GRADE

21C206.2C

REG NO: | | | | | | | | |

END TERM EXAMINATION JUNE 2023
BCA - II SEMESTER
GC206.2C: COMPUTER ARCHITECTURE

Duration: 2 Hours **Max Marks: 60**

Instruction: *Answers should be written in **English** only.*

PART-A

Answer **any EIGHT** questions. **Each** question carries **TWO** marks. **(8 X 2 = 16)**

1. Convert 10101111_2 to hexadecimal.
2. Find 2's complement of 10101.
3. What is General Instruction format of a computer?
4. What is accumulator?
5. What is RTL?
6. Write the format of control word.
7. Explain the types of bus in Computer Architecture.
8. List any a) Two input devices and b) Two output devices
9. What do you mean by Hit Ratio?
10. Explain RAID.

PART-B

Answer **any FOUR** questions. **Each** question carries **SIX** marks. **(4 X 6 = 24)**

1. Define and explain half adder with truth table and logic diagram.
2. Simplify using K-Map F(a,b,c,d) = $\sum(0,1,2,3,6,10,14)$.
3. Explain Registers of a Basic Computer.
4. Explain Instruction formats based on address by considering following example.
   $X = (A + B) * (C + D)$.
5. Explain Address Sequencing concept with neat diagram.
6. Explain any two types of mapping techniques in cache memory.

PART-C

Answer **any TWO** questions. **Each** question carries **TEN** marks. **(2 X 10 = 20)**

1. Construct a sequential Circuit for the following equations.
   Input: $D_A = A'X + BX$
   $D_B = AX'$
   Output: Y= AX+BX
2. Describe Data transfer and manipulation instructions with example.
3. Explain General Bus organization for seven CPU registers.
4. Explain DMA controller in detail.

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